WHAT IS CLAIMED IS:

1. A method for clamping a semiconductor wafer to an electrostatic chuck, comprising:

determining a single-phase square wave clamping voltage for the electrostatic chuck, wherein the determination is based, at least in part, on an inertial response time of the wafer;

placing the wafer on the electrostatic chuck, wherein a gap is defined between the wafer and the electrostatic chuck;

applying the determined single-phase square wave clamping voltage to the electrostatic chuck, therein electrostatically clamping the wafer to the electrostatic chuck; and

stopping the determined single-phase square wave clamping voltage, therein de-clamping the wafer from the electrostatic chuck.

2. The method of claim 1, wherein the determined single-phase square wave clamping voltage is applied to one or more electrodes associated with the electrostatic chuck.

3. The method of claim 1, wherein the electrostatic chuck comprises a flat-plate electrostatic chuck surface comprising a dielectric layer, and wherein placing the wafer on the electrostatic chuck comprises placing the wafer on the dielectric layer.

4. The method of claim 1, wherein the electrostatic chuck comprises a MEMS-based electrostatic chuck surface comprising a plurality of microstructures, and wherein placing the wafer on the electrostatic chuck

comprises placing the wafer on the plurality of microstructures.

5. The method of claim 4, wherein the plurality of microstructures provide a substantially uniform surface upon which the wafer is placed, and wherein the gap is significantly uniform across the electrostatic chuck.

6. The method of claim 1, further comprising applying a cooling gas backpressure on the wafer through the electrostatic chuck, wherein the determined single-phase square wave clamping voltage is further determined based on the cooling gas backpressure.

7. The method of claim 6, wherein the determined single-phase square wave clamping voltage is defined by a waveform having a rise time, a pulse width, and a pulse repetition frequency, and wherein the waveform is a function of an *RC* time constant associated with the electrostatic chuck, the wafer, an inertial response time of the wafer, and the cooling gas backpressure.

8. The method of claim 1, wherein determining the single-phase square wave clamping voltage further comprises determining a rise time of the determined single-phase square-wave clamping voltage, wherein the rise time is approximately less than the wafer inertial response time.

9. The method of claim 1, wherein the determined single-phase square wave clamping voltage causes a movement of the wafer away from the electrostatic chuck when the square wave crosses 0 volts, and wherein the movement is less than one tenth of the gap between the wafer and the electrostatic chuck.

10. The method of claim 1, wherein a pulse width of the determined single-phase square wave clamping voltage is shorter than a required de-clamping time which satisfies process throughput specifications.

11. The method of claim 1, wherein a pulse width of the determined single-phase square wave clamping voltage is longer than the wafer inertial response time.

12. The method of claim 11, wherein the pulse width of the determined single-phase square wave clamping voltage is approximately 10 or more times longer than the wafer inertial response time.

13. A system for clamping a wafer, comprising:

an electrostatic chuck comprising one or more electrodes operable to provide an electrostatic clamping force between a surface thereof and the wafer, the electrostatic chuck further having an *RC* time constant and a repelling force which is generally opposite the clamping force associated therewith, wherein a predetermined escape distance is generally defined by an inertial response time of the wafer, wherein the inertial response time is further associated with the *RC* time constant of the electrostatic chuck; and

a power supply configured to provide a single-phase square wave clamping voltage to the one or more electrodes.

14. The system of claim 13, wherein a rise time of the single-phase square wave clamping voltage is approximately less than the inertial response time of the wafer.

15. The system of claim 13, wherein a pulse width of the single-phase square wave clamping voltage is shorter than a required de-clamping time which satisfies process throughput specifications.

16. The system of claim 13, wherein a pulse width of the single-phase square wave clamping voltage is longer than the inertial response time of the wafer.

17. The system of claim 16, wherein the pulse width of the determined single-phase square wave clamping voltage is approximately 10 or more times longer than the wafer inertial response time.

18. The system of claim 13, wherein the surface comprises a flat plate.

19. The system of claim 13, wherein the surface comprises a plurality of MEMS microstructures.

20. The system of claim 13, further comprising a cooling gas supply, wherein the cooling gas supply is operable to provide a cooling gas backpressure between the surface of the electrostatic chuck and the wafer, therein contributing to the repelling force.